## Specialist Diploma in Embedded Systems: ED5502 Spring 2019, Homework 3

This homework sheet counts for 5% of the module assessment.

Submission date: Wednesday, 13 March 2019 (Week 8)

**1. (STM32L476RG Internal buses)**

Refer to the document ‘en.DM00083560\_L476\_Ref\_Mab.pdf’ available on Sulis under Resources/Data Sheets, to find the following information (see Table 1, pages 77-81):

On what internal STM32L476 internal bus would you find the following on-chip peripheral devices:

* GPIOG
* USART1
* ADC2
* USART3
* TIM5

**2. (STM32L476RG Address map)**

(a) Use the document ‘en.DM00083560\_L476\_Ref\_Mab.pdf’ (Table 1) and Table 39, (pages 311-312) to find the physical memory addresses of the following register:

GPIOD\_BRR

(b) Use the document ‘en.DM00083560\_L476\_Ref\_Mab.pdf’ (Table 1) and Table 251, (pages 1398-1399) to find the physical memory addresses of the following register:

USART4\_TDR

**3. (STM32L476RG Internal buses and Clock Tree)**

Write a line of C code to enable the Clock used for USART3. Hint: use one of the RCC\_xxxENR registers, see ‘en.DM00083560\_L476\_Ref\_Mab.pdf’, pages 249-259. (Hint: Table 1 will help to identify the correct RCC\_xxxENR register to use.)

**4. (USART Baud Rate)**

(a) Referring to the Power Point Slides, ES\_ARM\_L5\_Clocks\_and USART.pptx, slides 28-31, or to the Reference Manual, calculate the value of the USARTDIV field to set a Baud Rate of 57600 Baud, assuming a clock frequency of 40 MHz and that 16 times oversampling has been enabled.

(b) Suppose you are using USART4. Write a line of code to set the USART4 Baud Rate to 57600 Baud, based on the assumptions and calculations of (a) above.

**5. (Using the USART, polling mode)**

Referring to Power Point Slides, ES\_ARM\_L5\_Clocks\_and USART.pptx, slide 25, or to the Reference Manual, write a fragment of C code as follows:

Implement a wait loop that reads the USART3 ISR register, checking the TXE bit, which will wait until the TDR register is empty

Then write the data in the variable ‘new\_char’ to USART3 TDR register.

(Hint: the program examples on Sulis can be used as a template for this operation).

**Submission:**

Please submit your answers on Sulis before 5pm Wed 13 March 2019, in plain text, MS Word, pdf or any other readable format.

All questions carry equal marks.